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MOSFET DEVICE WITH A STRAINED CHANNEL

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a method used to fabricate a metal oxide semiconductor field effect transistor (MOSFET) device on an insulator layer, featuring a strained channel.

(2) Description of Prior Art

In order to suppress short channel effects as the gate length of metal oxide semiconductor field effect transistor (MOSFET) devices are scaled down, higher body doping concentrations, thinner gate insulator layers, and shallower source/drain doping profiles are necessary. Such requirements have become difficult to meet when conventional device structures based on bulk silicon substrates are employed. The heavy channel doping required to provide adequate suppression of short channel effects result in degraded mobility and enhanced junction leakage. In addition the reduction of gate insulator thickness, to minimize short channel effects, leads to direct tunnelling gate leakage current as well as raising concerns regarding gate insulator reliability.

A method of suppressing short channel effects is the formation of a MOSFET device

featuring an ultra thin silicon layer as the channel region, located on an insulator structure. In this type of structure the source to drain current is restricted to flow only in the region close to the gate, in the ultra thin channel silicon layer, grown to a thickness typically less than 200 Angstroms. Since this configuration does not rely on a heavily doped channel region for suppression of short channel effects it avoids the problems of mobility degradation due to impurity scattering and threshold voltage fluctuation due to random variation of the number of dopant atoms in the channel region. As a ultra thin source/drain region would contribute high series resistance a raised source/drain structure can be employed to avoid the series resistance problem.

Performance optimization of an ultra thin body MOSFET device is possible through the use of a strained channel region, where the strain modifies the band structure of the channel region resulting in enhanced carrier transport properties. However the implementation of a MOSFET device on an insulator structure, featuring a strained channel region is difficult to achieve via conventional processes, and therefore not previously addressed. The present invention will however describe a novel fabrication process sequence is which a silicon channel region, under biaxial tensile strain, is successfully employed as a component for a MOSFET device, where the silicon channel region is located in a thin silicon layer which in turn is located on an insulator structure. Prior art such as: Kibbel et al, in U.S. Pat. No. 6,313,016; Liaw et al, in U.S. Pat. No. 5,891,769; Chu et al, in U.S. Pat. No. 5,906,951; Fitzgerald et al, in U.S. Pat. No, 6,291,321; and Leoues et al, in U.S. Pat. No. 5,659,187; have described methods of forming strained semiconductor and semiconductor alloys, on insulator structures. These prior

arts however do not describe the novel process sequence used in this present invention, in which a thin, strained silicon layer is obtained on an underlying insulator structure.

SUMMARY OF THE INVENTION

It is an object of this invention to form a strained channel on an insulator structure, for use in an ultra-thin body MOSFET device. .

It is another object of this invention to form a strained channel in a silicon layer under biaxial tensile strain, obtained via growth of the silicon layer on an underlying relaxed layer or substrate with a natural lattice constant larger than that of silicon.

It is still another object of this invention to bond a first wafer comprised with the silicon strained channel, to a second wafer comprised with an insulator structure, followed by a cleaving procedure removing the underlying relaxed layer from the first wafer and resulting in a third wafer comprised of the strained silicon channel (from first wafer) on an insulator structure (from second wafer).

In accordance with the present invention a method of forming an ultra thin MOSFET device on an insulator structure, featuring a strained channel, is described. A first wafer comprised of a semiconductor alloy layer, such as silicon - germanium (SiGe), or silicon - germanium - carbon (SiGeC), with a lattice constant larger than that of silicon, is formed on an underlying semiconductor substrate. With the semiconductor in a relaxed state, a thin silicon

layer is epitaxially grown resulting in a first wafer comprised of a thin silicon layer overlying the underlying semiconductor alloy layer, on the semiconductor substrate. A second wafer comprised of an insulator layer on a semiconductor substrate is prepared and then bonded to the first wafer resulting in a third wafer featuring the thin silicon layer of the first wafer directly overlying the insulator layer of the second wafer. A cleaving procedure is employed to separate the thin silicon layer from the underlying semiconductor alloy layer of the first wafer, resulting in a fourth wafer with the desired configuration of the thin silicon layer from the first wafer, under biaxial tensile strain, located on the insulator layer which in turn is located on the underlying semiconductor substrate from the second wafer. Formation of a gate insulator layer on the thin silicon layer, is followed by definition of a gate structure. Formation of insulator spacers on the sides of the gate structure, and growth, or definition of a raised source/drain structure, complete the fabrication of a ultra thin MOSFET device, featuring a silicon channel region under biaxial tensile strain, on an underlying insulator structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 6, which schematically, in cross-sectional style, describe key stages used to fabricate an ultra thin MOSFET device, featuring a silicon channel region under biaxial tensile strain, located directly on an underlying insulator structure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating a MOSFET device, featuring a thin silicon channel under biaxial strain, located on an underlying insulator structure, will now be described in detail. A first semiconductor substrate 1, comprised of single crystalline silicon, with a <100> crystallographic orientation, is provided and shown schematically in Fig. 1. A material comprised with a natural lattice constant greater than that of silicon is next formed on first semiconductor substrate 1. The natural lattice constant of a material is its lattice constant in the relaxed state. Layer 2, a material with a natural larger lattice constant than that of silicon, can be a silicon - germanium (SiGe), layer, or a silicon - germanium - carbon (SiGeC) layer. The SiGe option is accomplished via epitaxial growth at a temperature between about 400 to 800° C, using silane, or disilane as a source for silicon, while using germane as a source for germanium. The thickness of SiGe layer 2, is between about 0.1 to 10 microns, with a fraction of germanium between about 0.05 to 0.8. The growth conditions used for layer 2, result in a relaxed SiGe layer on silicon semiconductor substrate 1. If desired layer 2, can be comprised of SiGeC, again obtained via epitaxial growth conditions at a temperature between about 400 to 800° C. Again silane, or disilane, and germane are used as reactants, with the addition of a hydrocarbon as a source for carbon. Layer 2, comprised of SiGeC, at a thickness between about 0.1 to 10 microns, is comprised with a germanium content between about 5 to 80 %, and with a carbon content between about 0 to 4 %, with the SiGeC layer again being in a relaxed condition. Therefore first wafer 100, shown schematically in Fig. 1, is now comprised of a relaxed layer 2, on semiconductor substrate 1.

Layer 3, comprised of a strained layer of silicon, is next epitaxially grown on the top surface of relaxed layer 2. Silicon layer 3, is grown at a temperature between about 400 to 800° C, using silane or disilane as a silicon source. Layer 3, or strained silicon layer 3, is grown to a thickness between about 20 to 1000 Angstroms. First wafer 100, shown schematically in Fig. 2, is now comprised of strained silicon layer 3, on relaxed semiconductor alloy layer 2, on silicon semiconductor substrate 1. The lattice constant of layer 2, is larger than that of strained silicon layer 3.

Second semiconductor 4, comprised of P type single crystalline silicon, with a <100> crystallographic orientation, is used as the substrate for second wafer 200, shown schematically in Fig. 3. Insulator layer 5, such as silicon dioxide, is next thermally grown on second semiconductor substrate 4, at a thickness between about 500 to 5000 Angstroms, via thermal oxidation procedures, performed at a temperature between about 800 to 1100° C, in an oxygen - steam ambient. Insulator layer 5, can also be a silicon oxide layer, obtained via low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD), procedures, at a thickness between about 500 to 5000 Angstroms, using tetraethylorthosilicate (TEOS), as a source. In addition, if desired insulator layer 5, can be comprised of silicon nitride, obtained at a thickness between about 500 to 5000 Angstroms, using silane and ammonia as reactants. Second wafer 200, is now comprised of insulator layer 5, on semiconductor substrate 4. Bonding of first wafer 100 to second wafer 200, is next performed using wafer bonding procedures, resulting in third wafer 300, comprised of semiconductor substrate 4, insulator layer 5, strained silicon layer 3, semiconductor alloy layer 2, and

semiconductor substrate 1. The wafer bonding procedure can be a direct bonding process. In the direct bonding process, two ultra clean wafers are mated at room temperature followed by subsequent anneal to increase the bond strength. The bond strength increases with the annealing temperature which can be between about 200 to 1100° C. This is schematically shown in Fig. 3.

Referring to third wafer 300, a large strain gradient exists at the interface between strained silicon layer 3, and relaxed semiconductor alloy, or SiGe layer 2. The large strain gradient allows a cut or a cleave to be accomplished at this interface resulting in the desired SOI configuration presented by fourth wafer 400, comprised of strained silicon layer 3, on insulator layer 5, with the SOI region residing on semiconductor substrate 4. The combination of a thin silicon layer, under biaxial tensile strain, on an insulator layer, provides the configuration needed to fabricate the ultra thin MOSFET device featuring enhanced carrier mobility in the stained channel region, with a reduced risk of short channel effects a result of the thin silicon layer overlying an insulator layer. This is schematically shown in Fig. 4. Remaining fifth wafer 500, now comprised of semiconductor alloy layer 2, on semiconductor substrate 1, can be reclaimed and reused if desired. The cleaving procedure is done by providing energy to the interface between strained silicon layer 3, and relaxed semiconductor alloy, or SiGe layer 2, such as using compressed air, pressurized fluid, or water jet. This is a controlled cleaving action at the interface whereupon the cleaving action is made using a propagating cleave front to separate the strained silicon layer 3, from the relaxed semiconductor alloy, or SiGe layer 2.

The fabrication of the ultra thin MOSFET device, on fourth wafer 400, featuring an SOI structure which in turn features a thin, strained silicon component, is next described and schematically illustrated using Figs. 5 - 6. Gate insulator layer 6, comprised of silicon dioxide is obtained at a thickness between about 5 to 50 Angstroms, via thermal oxidation procedures performed at a temperature between about 600 to 1000° C, in an oxygen - steam ambient. The thermal growth of silicon dioxide gate insulator layer 6, consumes a top portion of strained silicon layer 3. Gate structure 7, comprised of polysilicon, or a polycide (metal silicide on polysilicon), is next formed via deposition of a polysilicon, (or a metal silicide - polysilicon), layer, via LPCVD procedures, to a thickness between about 500 to 2000 Angstroms. The polysilicon, or the polysilicon component of the polycide layer, can be doped in situ during deposition via the addition of arsine, or phosphine to a silane ambient, or the polysilicon or polysilicon component of the polycide layer, can be deposited intrinsically then doped via implantation of arsenic or phosphorous ions. The metal silicide layer, such as a cobalt silicide layer, used with the polycide option, can be deposited via LPCVD procedures after the polysilicon component has been deposited and doped. A photoresist shape, not shown in the drawings, is next used as a mask to allow an anisotropic, reactive ion etching (RIE) procedure, to define gate structure 7, shown schematically in Fig. 5. The RIE procedure is performed using Cl_2 or SF_6 as a selective etchant for polysilicon or polycide. Removal of the photoresist shape, used for definition of gate structure 7, is accomplished using plasma oxygen ashing procedures, followed by a wet clean procedure. The wet clean procedure employs a buffered hydrofluoric acid dip, which removes the portions of silicon dioxide gate insulator layer 6, not covered by gate structure 7.

If a source/drain region were to only be formed in the thin strained silicon layer high series resistance degrading drive current would occur. Therefore to avoid these deleterious effects a raised source/drain structure is formed and schematically shown in Fig. 6. First, insulator spacers 8, are formed on the sides of gate structure 7, via deposition of an insulator layer such as silicon oxide, or silicon nitride. The silicon oxide or silicon nitride layer is obtained via LPCVD or PECVD procedures, at a thickness between about 100 to 1000 Angstroms. Another selective, anisotropic RIE procedure is employed, using CHF_3 or CF_4 as a selective etchant for the insulator layer, resulting in the formation of insulator spacers 8, on the sides of gate structure 7. Formation of raised source/drain structure 9, is addressed, using either a deposited, then etched polysilicon option, or a selectively grown single crystalline silicon option. A first option employs the selective growth of single crystalline silicon, originating from the top surface of exposed portions of strained silicon layer 3, and extending to a height of between about 50 to 1000 Angstroms. The selective silicon growth does may or may not occur on the top surface of polysilicon gate structure 7. Raised silicon source/drain structure 9, is doped in situ during deposition, or grown intrinsically then doped via ion implantation procedures. The polysilicon option begins with a deposition of a polysilicon layer, via LPCVD procedures, to a thickness between about 500 to 4000 Angstroms, at a thickness greater than the height of gate structure 7. The polysilicon layer can either be doped in situ during deposition via the addition of arsine, or phosphine to a silane ambient, or the polysilicon layer can be deposited intrinsically than subjected to implantation of arsenic or phosphorous ions. An etch back procedure, using Cl_2 or SF_6 as an etchant for polysilicon, is used to define raised polysilicon source/drain structures 9. The etch back

procedure is terminated at the appearance of the top of insulator spacers 8.

The incorporation of the thin strained silicon layer, featuring biaxial tensile strain, results in enhancement of electron transport properties for the N channel device described in this invention. However if desired a P type channel device can also be formed using the thin strained silicon layer, allowing the enhancement of hole transport properties to be realized via use of the biaxial tensile strained region. If the P type channel device is desired, raised source/drain structures 9, would be doped P type, in addition to the P type doping of gate structure 7.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is: